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DICKSTEIN SHAPIRO LLP
1825 EYE STREET NW
Washington, DC 20006-5403

EXAMINER	
MYERS, PAUL R	
ART UNIT	PAPER NUMBER
2111	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/02/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary for Applications Under Accelerated Examination	Application No.	Applicant(s)	
	10/730,896	PAWLOWSKI, J. THOMAS	
	Examiner	Art Unit	
	Paul R. Myers	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Since this application has been granted special status under the accelerated examination program, NO extensions of time under 37 CFR 1.136(a) will be permitted and a SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE:

ONE MONTH OR THIRTY (30) DAYS, WHICHEVER IS LONGER,
FROM THE MAILING DATE OF THIS COMMUNICATION – if this is a non-final action or a *Quayle* action.
(Examiner: For **FINAL** actions, please use PTOL-326.)

The objective of the accelerated examination program is to complete the examination of an application within twelve months from the filing date of the application. Any reply must be filed electronically via EFS-Web so that the papers will be expeditiously processed and considered. If the reply is not filed electronically via EFS-Web, the final disposition of the application may occur later than twelve months from the filing of the application.

Status

1)☒ Responsive to communication(s) filed on *01 January 1964*.

2)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

3)☐ Claim(s) _____ is/are pending in the application.
3a) Of the above claim(s) _____ is/are withdrawn from consideration.

4)☐ Claim(s) _____ is/are allowed.

5)☒ Claim(s) *1-64* is/are rejected.

6)☐ Claim(s) _____ is/are objected to.

7)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

8)☐ The specification is objected to by the Examiner.

9)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

10)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

11)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a)☐ All b)☐ Some * c)☐ None of:
1.☐ Certified copies of the priority documents have been received.
2.☐ Certified copies of the priority documents have been received in Application No. _____.
3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

- See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 1/24/07 have been fully considered but they are not persuasive.

In regards to applicants argument that none of Curran, Burleson, or de la Iglesia et al teach the newly claimed "capturing a state of previously transmitted bits on the bidirectional bus with a first clocked register according to a clock signal, capturing a state of an inversion bit associated with the previously transmitted bits with a second clocked register according to the clock signal and determining from the captured state of the previously transmitted bits whether the first bits should be inverted": Curran teaches figure 6 a register 186 that is inherently clocked (current and next bus cycles used) which is logically separated into to regions the previous data region and the S inversion bit region see the bole separating line. MPEP 2144.04 V C indicates that to make separate is not a patentable distinction. Burleson et al teaches figure 8 a 9 bit latch that includes both the 8 bit data and the inversion bit. Latches can be either clocked of non-clocked. Official notice is taken that clocked latches are used for synchronization. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use a clocked latch/register because this would have allowed for data synchronization. De la Iglesia et al teaches two separate registers one or more for the data and one for the plurality of inversion bits (see figures 2A-2D). These registers are inherently clocked. The examiner notes applicant did not address the secondary reference to Devanney et al which expressly shows separate data and inversion bit registers that are clocked.

In regards to applicants argument that Curran, Burleson, and de la Iglesia are silent with respect to "outputting on a separate line[] with a clocked register according to a clock signal, the inversion bit": The examiner has already addressed the issue of a clock. With respect to outputting on a separate line Curran teaches the data and the inversion bit being outputted on bus 188. Bus 188 is a parallel bus made up of data and the inversion bit. The inversion bit is on a separate line. Burleson expressly shows the data on lines D0-D7 and the inversion bit on line inv. De la Iglesia expressly shows (Figure 5) 8 separate inversion bit lines and 64 data bit lines.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

In response to Applicant's argument that there is no suggestion to combine the references, the Examiner recognizes that references cannot be arbitrarily combined and that there must be some reason why one skilled in the art would be motivated to make the proposed combination of primary and secondary references. In re Nomiya, 184 USPQ 607 (CCPA 1975). However, there is no requirement that a motivation to make the modification be expressly articulated. The test for combining references is what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. In re McLaughlin, 170 USPQ 209 (CCPA 1971). references

are evaluated by what they suggest to one versed in the art, rather than by their specific disclosures. In re Bozek, 163 USPQ 545 (CCPA) 1969.

The test of obviousness is:

"whether the teachings of the prior art, taken as a whole, would have made obvious the claimed invention," *In re Gorman*, 933 F.2d at 986, 18 USPQ 2d at 1888.

> Subject matter is unpatentable under section 103 if it "'would have been obvious . . . to a person having ordinary skill in the art.' While there must be some teaching, reason, suggestion, or motivation to combine existing elements to produce the claimed device, it is not necessary that the cited references or prior art specifically suggest making the combination." *In re Nilssen*, 851 F.2d 1401, 1403, 7 USPQ 2d 1500, 1502 (Fed. Cir. 1988).
>
> "Such suggestion or motivation to combine prior art teachings can derive solely from the existence of a teaching, which one of ordinary skill in the art would be presumed to know, and the use of that teaching to solve the same [or] similar problem which it addresses." *In re Wood*, 599 F.2d 1032, 1037, 202 USPQ 171, 174 (CCPA 1979).
>
> "In sum, it is off the mark for litigants to argue, as many do, that an invention cannot be held to have been obvious unless a suggestion to combine prior art teachings is found *in* a specific reference."
>
> Entire quote from *In re Oetiker*, 24 USPQ 2d 1443 (CAFC 1992).

Accordingly, it is not required to disclose or specifically suggest particular elements. Instead the measure is what the teachings would suggest to one of ordinary skill in the art, not what the art specifically suggests.

"Not only the specific teachings of a reference but also reasonable inferences which the artisan would have logically drawn therefrom may be properly evaluated in formulating a rejection." *In re Preda*, 401 F.2d 825, 159 USPQ 342 (CCPA 1968) and *In re Shepard* 319 F.2d 194, 138 USPQ 148 (CCPA 1963).

"Furthermore, artisans must be presumed to know something about the art apart from what the references disclose." *In re Jacoby*, 309 F.2d 513, 135 USPQ 317 (CCPA 1962). Such as for example that registers are clocked.

"The conclusion of obviousness may be made from common knowledge and common sense of a person of ordinary skill in the art without any specific hint or suggestion in a particular reference." *In re Bozek*, 416 F.2d 1385, 163 USPQ 545 (CCPA 1969).

"Every reference relies to some extent on knowledge of persons skilled in the art to complement that which is disclosed therein." *In re Bode*, 550 F.2d 656, 193 USPQ 12 (CCPA 1977).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim1-13, 17-22, 26-36, 38-49, 51-64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Curran PN 5,574,921 in view of Devanney et al PN 6,243,779.

In regards to claims 1, 17, 26, 48, 63-64: Curran teaches a method of performing bus inversion on first bits (181) to be transmitted on a bus (188), from a first device (the sending device) to a second device (the receiving device), said method comprising the steps of: determining whether the first device will drive output data during a next drive cycle (the first device will drive during the next drive cycle. Note some form of arbitration which would include always granting or some other form is inherent.); if it is determined that the first device will drive output data during the next cycle; capturing a state of previously transmitted bits on the bus (186 nbits); capturing a state of an inversion bit associated with the previously transmitted bits (186 sbit); and determining from the captured state of the previously transmitted bits (186 nbits) whether the first bits should be inverted (via 183 184 and 185). Curran's bus is parallel which includes separate lines. Curran is silent upon whether bus 188 is a unidirectional or bidirectional bus. Devanney et al expressly teaches that bit inversion can either unidirectional or bidirectional (Column 2 lines 21-22). It would have been obvious to use Curran's bit inversion on either a unidirectional or bidirectional bus because this would have prevented unduly limiting the usability of Curran's system. Even though Curran inherently clocks the data, Devanney expressly shows that data is clocked.

In regards to claims 2, 27, 49: Curran teaches inverting the bits if it is determined the bits should be inverted (via 185).

In regards to claims 3-4, 9, 21, 28-29, 33: Curran teaches outputting the inverted/not inverted first bits on the bus; and outputting the inversion bit with a value indicating that the first bits have been inverted/not inverted.

In regards to claims 5, 18, 30: Curran teaches inverting if the hamming distance is greater than ½ the number of bits.

In regards to claims 6, 19, 31: Curran teaches taking into account the inversion bit. Curran does not teach computing the hamming distance than taking into account the inversion bit instead Curran teaches taking into account the inversion bit than computing the hamming distance. However in Curran when taking into account the inversion bit, if the hamming distance of the data equal ½ the number of bits than the only bit remaining is the inversion bit. Thus if the value of the inversion bit is 1 than the over all hamming distance will be greater than ½ and the next inversion bit will be set to 1. If the value of the inversion bit is 0 than the over all hamming distance will be less than ½ and the next value of the inversion bit will be set to 0. Thus if the hamming distance of the data is ½ than the next value of the inversion bit will be set to the previous value of the inversion bit. It would have been obvious to a person of ordinary skill in the art at the time of the invention to compute the hamming distance than take into account the inversion bit as a basic principal of math.

In regards to claim 7: Curran teaches the number of bits being N. 50% of all values of N are even.

In regards to claims 8, 20, 32: Curran teaches outputting the inverted/not inverted first bits on the bus; and outputting the inversion bit with a value indicating that the first bits have been inverted/not inverted.

In regards to claims 38-42, 51-54: Curran teaches inverting the "bus" Curran does not limit the type of bus. Curran is silent if the bus is the address, command or data bus. Official Notice is taken that address, data and command buses are well known types of buses. It would

have been obvious to a person of ordinary skill in the art at the time of the invention perform Curran's invention on any type of parallel bus because this would have provides for Curran's power savings without limiting the type of bus.

In regards to claim 62: Curran teaches the inversion as described above. Curran only expressly teaches two devices the sending and receiving devices. Curran does not expressly state that there can be more than 2 devices. Official notice is taken that systems with more than 2 devices are common. It would have been obvious to use Curran's bus inversion system in systems.

In regards to claim 10: Curran teaches the number of bits being N. 50% of all values of N are odd.

In regards to claims 11, 34: Curran captures the bits only when bits are available to be transferred.

In regards to claims 12, 35: Curran captures the bits on every transfer.

In regards to claims 13, 22, 36: Curran makes the determination for reducing the number of transitions of the first bits and the inversion bit.

In regards to claims 43-47, 55-60: Curran teaches the number of bits being N. 4,8,9,16 and 32 are included in N.

In regards to claim 61: Curran teaches multiple inversion bits.

4. Claims 1-13, 17-22, 26-36, 38-49, 51-64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bus-Invert Coding for low-power I/O by M.R. Stan and W.P. Burleson herein after Burleson in view of Devanney et al PN 6,243,779.

In regards to claims 1, 17, 26, 48, 63-64: Burleson teaches a method of performing bus inversion on first bits (D0-D7 or sub-buses section III C.) to be transmitted on a bus (bus), from a first device (the sending device) to a second device (the receiving device), said method comprising the steps of: determining whether the first device will drive output data during a next drive cycle (the first device will drive during the next drive cycle. Note some form of arbitration including always granted is inherent.); if it is determined that the first device will drive output data during the next cycle; capturing a state of previously transmitted bits on the bus (Pages 53-54 steps 1-4); capturing a state of an inversion bit associated with the previously transmitted bits (invert and description of figure 6)); and determining from the captured state of the previously transmitted bits (D0-D7) whether the first bits should be inverted (steps 1-4). Burleson is silent upon whether the bus is a unidirectional or bidirectional bus and whether the data and inversion bits are clocked. Devanney et al expressly teaches that bit inversion can either unidirectional or bidirectional (Column 2 lines 21-22) and clocking the data/inversion bit. It would have been obvious to use Burleson's bit inversion on either a unidirectional or bidirectional bus because this would have prevented limiting Burleson. It also would have been obvious to a person of ordinary skill in the art at the time of the invention to clock the data because this would have prevented errors due to timing skew.

In regards to claims 2, 27, 49: Burleson teaches inverting the bits if it is determined the bits should be inverted (step 2).

In regards to claims 3-4, 9, 21, 28-29, 33: Burleson teaches outputting the inverted/not inverted first bits on the bus; and outputting the inversion bit with a value indicating that the first bits have been inverted/not inverted.

In regards to claims 5, 18, 30: Burleson teaches inverting if the hamming distance is greater than ½.

In regards to claims 6, 19, 31: Burleson teaches taking into account the inversion bit. Burleson does not teach computing the hamming distance than taking into account the inversion bit. However Burleson is silent as to when to take into account the inversion bit, if the hamming distance of the data equal ½ the number of bits than the only bit remaining is the inversion bit. Thus if the value of the inversion bit is 1 than the over all hamming distance will be greater than ½ and the next inversion bit will be set to 1. If the value of the inversion bit is 0 than the over all hamming distance will be less than ½ and the next value of the inversion bit will be set to 0. Thus if the hamming distance of the data is ½ than the next value of the inversion bit will be set to the previous value of the inversion bit. It would have been obvious to a person of ordinary skill in the art at the time of the invention to compute the hamming distance than take into account the inversion bit as a basic principal of math.

In regards to claim 7: Burleson teaches the number of bits being N, in all examples the number of bits being even.

In regards to claim 8, 20, 32: Burleson teaches outputting the inverted/not inverted first bits on the bus; and outputting the inversion bit with a value indicating that the first bits have been inverted/not inverted.

In regards to claims 40, 53: Burleson teaches inverting the data and address buses. Burleson does not limit the type of bus. Official Notice is taken that address, data and command buses are well known types of buses. It would have been obvious to a person of ordinary skill in

the art at the time of the invention perform Burleson's invention on any type of parallel bus because this would have provides for Burleson's power savings without limiting the type of bus.

In regards to claim 62: Burleson teaches the inversion as described above. Burleson does not expressly state that there can be more than 2 devices. Official notice is taken that systems with more than 2 devices are common. It would have been obvious to use Burleson's bus inversion system in systems

In regards to claim 10: Burleson teaches the number of bits being N. 50% of all values of N are odd.

In regards to claims 11, 34: Burleson captures the bits only when bits are available to be transferred.

In regards to claims 12, 35: Burleson captures the bits on every transfer.

In regards to claims 13, 22, 36: Burleson makes the determination for reducing the number of transitions of the first bits and the inversion bit.

In regards to claims 38-39, 51-52: Burleson teaches the bus can also be the address bus.

In regards to claims 41-42, 54: Burleson teaches the bus can be the data bus.

In regards to claims 43-47, 55-60: Burleson teaches the number of bits being N. 4,8,9,16 and 32 are included in N.

In regards to claim 61: Burleson teaches multiple inversion bits.

5. Claims 1, 13-17, 22-26, 36-37, 48, 50, 63-64 are rejected under 35 U.S.C. 103(a) as being unpatentable over de la Iglesia et al PN 6,490,703 in view of Devanney et al PN 6,243,779.

In regards to claims 1, 17, 26, 48, 63-64: de la Iglesia et al teaches a method of performing bus inversion on first bits (Fig 2A-2D) to be transmitted on a bus, from a first device (the sending device) to a second device (the receiving device), said method comprising the steps of: determining whether the first device will drive output data during a next drive cycle (the first device will drive during the next drive cycle. Note some form of arbitration including always granted is inherent.); if it is determined that the first device will drive output data during the next cycle; capturing a state of previously transmitted bits on the bus (Hamming code), capturing a state of an inversion bit associated with the previously transmitted bits (Flip); and determining from the captured state of the previously transmitted bits whether the first bits should be inverted. de la Iglesia et al is silent upon whether the bus is a unidirectional or bidirectional bus. Devanney et al expressly teaches that bit inversion can either unidirectional or bidirectional (Column 2 lines 21-22). It would have been obvious to use de la Iglesia et al's bit inversion on either a unidirectional or bidirectional bus because this would have prevented limiting the usability of de la Iglesia et al's system.

In regards to claims 13, 22, 36: de la Iglesia et al teaches the determination for reducing the number of transitions of the first bits and the inversion bit (POLF).

In regards to claims 14, 23, 37, 50: de la Iglesia et al teaches the determination for reducing the number of bits having a predetermined logic state (POLS).

In regards to claims 15, 24: de la Iglesia et al teaches the state being a logical 1.

In regards to claims 16, 25: de la Iglesia et al teaches the predetermined logic state being a logical 1. Official Notice is taken that negative logic is well known. It would have been obvious to have the predetermined logic state to be a logical 0 because this would have

accounted for systems in which logical 0 consumes more power than logical 1 such as negative logic.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Several prior art references are provided teaching bus inversion:

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul R. Myers whose telephone number is 571 272 3639. The examiner can normally be reached on Mon-Thur 6:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (571) 272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PRM
February 28, 2007

PAUL R. MYERS
PRIMARY EXAMINER